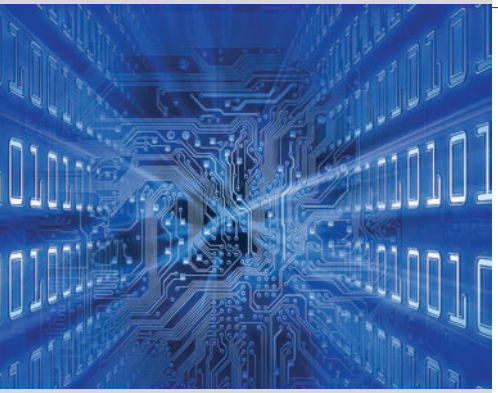
PROJECT RESULT

EDA for SOC Design and DFM

MEDEA+

2A714: Hardware-dependent software for systems on chip (SoftSoC)



Boosting flexible hardware and software design for system-on-chip devices

The MEDEA+ SoftSoC project has developed hardware-dependent software solutions to help system designers in the integration of hardware blocks in a wide range of electronic systems. The approach is based on proposed extensions to the IP-XACT standard and makes it possible to speed the design of new systems in a wide range of sectors, including telecommunications, automotive and consumer electronics. SoftSoC solutions will enable Europe to maintain leadership in key strategic markets by increasing the capacity of system-on-chip designers to build larger and better quality systems in less time.

By far the majority of advanced electronic products are now based on system-on-chip (SoC) solutions consisting of a highly integrated semiconductor chip with complementary software for controlling the hardware intellectual property (IP) blocks. Designing, building, configuring, integrating and testing this hardware-dependent software (HDS) has become a huge task, resulting in a major productivity bottleneck in SoC systems.

The MEDEA+ 2A714 SoftSoC project set out to eliminate this bottleneck by a systematic and highly-automated approach to combining hardware IP blocks with the embedded HDS in efficient design packages. The method developed enables efficient and automated integration of hardware and software IP into new SoC devices.

Reducing time to market

SoftSoC worked on reducing time to market in several ways, starting with the development of methods for systems integration based on use of the IP-XACT XML standard. This standard aims at describing the hardware topology of a subsystem, making it possible for customers to integrate this description into their own design tools and to take it into account automatically when assembling their systems.

The MEDEA+ project set out to extend the IP-XACT standard with new features; the proposals for extensions came from partner NXP, a major European chipmaker which had strong experience in this field. The main idea was provide a new description method enabling integration of hardware IP and the lowest level of software. Such an approach makes possible a degree of integration of hardware and software subsystems in a product.

At the same time, SoftSoC sought to improve software quality – specifically that of low level software. The description of the software based on IP-XACT could be used to improve quality through design automation with new tools for software generation. The result is both improved quality and lower cost.

Improving system integration

SoftSoC involved system composition rather than real IP design with the objective of improving system integration and helping customers to use systems. Work was carried out on simulation technologies to develop system-exploration technologies. Partners created tools to generate simulators to exploit IP-XACT databases. By changing the descriptions of a system, it was possible to assess the impact of the modifications with the simulators.

Tools and methodologies developed made it possible to:

- Provide automated configuration, integration and verification of system IP made up of

both hardware and HDS components on the SoC platform;
- Provide a high level view of hardware resources to facilitate development of the middleware and application software; and
- Generate correct and efficient IP concepts, including composition into subsystems and verification setups.

Some 13 tools were developed during the project by the various partners exploiting the IP-XACT kind of description to improve embedded systems covering modelling, simulation, implementation, validation and deployment domains.

Innovations included:

- IP modelling breakthroughs in HDS architecture, with IP views for integration, exploration and verification including consistent variability management of hardware and HDS;
- IP integration breakthroughs with architecture and methodology based on compositional IP modelling and use-case demonstrators indicating a 10 to 30% reduction in costs;
- HDS design automation breakthrough with IP configuration and generation tools, design-space exploration tools and system-configuration, generation and test tools; and
- Standardisation breakthroughs with continuing IP-XACT extensions standardisation, based on IP modelling results.

Range of organisations involved

A wide range of organisations was involved in this MEDEA+ project. NXP and Synopsis were the biggest partners; both are involved in the design of embedded systems with IP-XACT at the heart of their development processes. Working on the extension of the standard has helped them to improve their efficiency.

Academic partners worked on the technology and scientific aspects. The TIMA-INPG laboratory in France developed open-source technologies which are already available on Internet for public use. Small and medium-sized enterprise (SME) partners and subcontractors were able to make innovations in the technologies related to IP-XACT, allowing them to improve their own offerings based on the results of SoftSoC.

While the industrial partners may have no products on the market yet, they are using the project results in their own production. They also worked on standardisation with several extensions to IP-XACT in progress. These extensions still need to reach tool providers and this could take one to two years. However, all partners are ready to use the innovations but need industrialisation of the results with new tools and services.

Applications will be across many industries. Project partners targeted their own specific areas. For example, Thales focused on integrating hardware blocks for its security products and telecommunications systems, while Thomson Video Networks sought improvements for applications such as TV set-top boxes. NXP targeted areas that included automotive electronics and smart-phone security.

Long-term impact

Overall, the proposed extension to the IP-XACT standard should have a long-term impact on industry. Thales for example has determined that it could save 30% of costs in the development phase of its embedded software as a result. SoftSoC results should also lead to an improvement in time to market. However it will require more industrialisation for wider use in Europe.

EDA for SOC Design and DFM

2A714: Hardware-dependent software for systems on chip (SoftSoC)

PARTNERS:

CEA-LETI
Compaan Design
DS2-Marvell
LIACS
Magillem Design Services
NXP Semiconductors
Synopsys
Thales
Thomson Video Networks
TIMA-INPG
TU Delft
Uni Cantabria

PROJECT LEADER:

Anne-Marie Fouilliart
Thales

KEY PROJECT DATES:

Start: June 2008
End: August 2011

COUNTRIES INVOLVED:

France
The Netherlands
Spain

CATRENE Office
9 Avenue René Coty
F-75014 Paris
France
Tel.: +33 1 40 64 45 60
Fax: +33 1 43 21 44 71
Email: catrene@catrene.org
http://www.catrene.org

EUREKA Σ!

MEDEA+ Σ!2365 is the industry-driven pan-European programme for advanced co-operative R&D in microelectronics to ensure Europe's technological and industrial competitiveness in this sector on a worldwide basis.

MEDEA+ focuses on enabling technologies for the Information Society and aims to make Europe a leader in system innovation on silicon.